Programmable AC Current Booster for Faster Edge-Rate Output in High Speed Applications

Field of The Invention

Embodiments of the present invention relate to achieving faster output signal edge rates in high frequency signaling for programmable logic devices (PLDs) and other integrated circuits (ICs), most particularly to signals which may be designed to conform to any one of several different high frequency input/ output (I/O) signaling standards.

Background of The Invention

Programmable logic devices (PLDs) are well known. Commonly, a PLD has a plurality of substantially identical logic elements, each of which can be programmed to perform certain desired logic functions. The logic elements have access to a programmable interconnect structure that allows a user to interconnect the various logic elements in almost any desired configuration. The interconnect structure also provides access to a plurality of I/O pins, with the connections of the pins to the interconnect structure also being programmable and being made through suitable I/O buffer or driver circuitry. The PLD may be field programmable or programmable, either wholly or partially, in any other manner. It may be one-time only programmable, or it may be reprogrammable. The term PLD as

used herein will be considered broad enough to include all such devices.

As user applications incorporating PLDs evolve to operate at yet higher and higher speeds, and higher frequency signaling standards evolve to support those requirements, it is desirable that the I/O capability of PLDs keep pace with these developments.

In order to achieve successful operation in circuits operating at high speeds, typically greater than 200Mhz at present, existing I/O signaling standards require a signal waveform having fast edge rate and small output voltage swing, in order to maintain precise phase relationships between the high frequency signals. These two crucial requirements, fast edge rate and small output voltage swing, are physical characteristics inherently in opposition with each other. Overdriving for a faster edge rate directly results in increased output voltage swing. It is therefore becoming increasingly difficult to meet both requirements when the same output current settings are used for both AC and DC states as circuit speeds continue to increase.

Summary of the Invention

An AC current booster is described herein capable of operating at high frequencies for high speed applications and is described in several embodiments including a single-ended output circuit and a differential output circuit. Although the signal frequencies are typically

around 200MHz in one embodiment, the present invention may be equally applicable to circuit speeds that are lower or higher. Embodiments of the present invention can be programmed to provide any specific combination of output current, capacitive loading, output voltage swing and signal edge rate (typically in the order of 100 picoseconds) in order to conform to any one of several well known I/O signaling standards.

Some examples of commonly known I/O standards which use single-ended signaling circuits include High Speed Transceiver Logic (HSTL) Classes 1 and 2, Series Stub Terminated Logic (SSTL) Classes 1 and 2, and Peripheral Component Interface (PCI). Embodiments of the present invention are compatible with these examples.

Other commonly known I/O standards which use differential signaling circuits include Low Voltage Differential Signaling (LVDS), HyperTransport (HT), and Low-Voltage Positive Emitter-Coupled Logic (LVPECL). Embodiments of the present invention are compatible with these examples.

Embodiments of the present invention allow for bifurcated control of the AC switching rate and the DC state of a given output signal, in order to achieve faster rising and falling edge rates without the undesirable increased output voltage swing. Fast edge rates require a large switching current to charge up the capacitive loading, while providing a small DC current to limit the output voltage swing. The programmable current booster described here provides a separate AC current during the output switching phase, while not affecting the DC current or the

output voltage swing. Importantly, the strength and the duration of the AC booster current are programmable to allow a user the maximum flexibility in conforming to any of the I/O signaling standards such as HSTL, SSTL, LVDS, LVPECL or HyperTransport, though the present invention is not limited to only those standards. Embodiments of the present invention may be equally applicable to other relevant existing standards as well as those standards which have yet to be proposed or fully developed.

Though not limited to implementation in PLDs, the embodiments of the present invention are particularly suited to PLD output drivers and output drivers for other programmable ICs. These devices tend to have more demanding I/O requirements as they are very commonly deployed in interfacing with many varied signaling standards.

Brief Description of the Drawings

FIG. 1 is a block diagram of an exemplary programmable current booster according to one embodiment of the present invention as applied to a single-ended output driver.

FIG. 2A is a preferred implementation of the single-ended output driver according to an embodiment of the present invention.

FIG. 2B illustrates a timing diagram of the single-ended output driver operation in the case with the DC output enabled.

FIG. 2C illustrates a timing diagram of the single-ended output driver operation in the case with the AC current booster enabled.

FIG. 3 is a preferred implementation of a differential output driver according to an embodiment of the present invention.

FIG. 4 shows exemplary details of the differential DC stage rising edge control circuit.

FIG. 5 shows exemplary details of the differential DC stage falling edge control circuit.

FIG. 6 illustrates a timing diagram of the differential output driver operation.

Detailed Description of the Invention

The term "rising edge" used in describing the embodiments of the present invention refers to the rising edge of the signal waveform as the signal voltage level transitions from a LOW to a HIGH state. Similarly, the term "falling edge" refers to the falling edge of the signal waveform as the signal voltage level transitions from a HIGH to a LOW state.

SINGLE-ENDED EMBODIMENT

FIG. 1 is a block diagram of the programmable current booster 100 according to one embodiment of the present

invention as applied to a single-ended output driver. During configuration of the PLD, configuration signals 103 and 104 ("enable signals") which originate from the PLD and are applied to the rising and falling edge control circuits 106 and 110 respectively. Bifurcated control of the rising edge of the single-ended output signal is applied via rising edge control circuitry 106 and rising edge output current control circuitry 108.

Similarly, the falling edge characteristics are conditioned and controlled via falling edge control circuitry 110 and a falling edge output current regulation circuitry 112 of Figure 1. The rising edge and falling edge control circuitry have a common input or data signal 102 which typically originates from the core of the PLD. The separately conditioned rising and falling edge characteristics of the input signal are eventually incorporated into a single signal output 114.

FIG. 2A illustrates an exemplary circuit diagram of the embodiment 100 of the present invention depicted in the block diagram of FIG. 1, and represents a preferred implementation of a single-ended output driver circuit. Single-ended drivers are used in the implementation of single-ended signals, e.g., signals that are referenced to ground.

Output transistors 220 and 224 are used to regulate the magnitude of the AC current and DC current. Transistor 220 is controlled by the output of OR gate 212. Transistor 224 is controlled by the output of AND gate 216. The duration of the current flowing through the output

transistors is programmable via the rising edge control circuit 106 and falling edge control circuit 110.

Common input signal 102 is typically inverted as applied to all circuits depicted in FIG. 2A. A configuration bit 202 controls operation of rising edge circuit 106. The configuration bit may be a RAM bit, but may also be implemented via one-time programmable device arrangements such as those based on programmable logic elements made from fuses or antifuses, or may be implemented via SRAM, DRAM, EPROM, EEPROM, MRAM or the like.

If configuration signal 104 is LOW, output transistor 220 is always off. When configuration signal 104 is HIGH, output transistor 220 is enabled, but the duration of its ON state is programmable in two ways. First, if RAM bit 202 is programmed to be HIGH, then output transistor 220 will remain ON as long as common input signal 102 is HIGH, thereby providing a continuous DC output current which would contribute to the output voltage swing. Second, if RAM bit 202 is configured to be LOW, then output transistor 220 will be ON only during the edge transition time when input signal 102 is switching from LOW to HIGH. The duration of this ON time is programmable via programmable delay element 206. This short period of current through output transistor 220 will charge up the loading on output pin 114, and reduce the rise time, but will not affect the DC output voltage swing.

Similarly, output transistor 224 can be totally disabled when configuration signal 103 is LOW, or can be programmed

to be ON as long as common input signal 102 is low, or can even be programmed to be ON only when common input signal 102 is switching from HIGH to LOW, thereby providing a DC output current. Configuration bit 204 controls operation of falling edge circuit 110. Programmable delay element 208 is similarly used to control the ON duration of output transistor 224.

Rising edge output transistor 220 is most efficiently implemented using PMOS construction in one embodiment, though it is not limited to such. On the other hand, inherent NMOS transistor characteristics favor their use in falling edge output transistor 224.

Additional parallel-coupled sets of control circuits can be connected in the cascaded manner shown for at least a second set of rising and falling edge circuitry 236, each such output set having varying channel width, thereby allowing users to program them into various combinations of DC and AC current paths. To control the strength of the current for the output signal 114, several output transistors may be connected in parallel. In this case, pull-up output transistors 220 and 232 are shown connected in parallel, and so are pull-down output transistors 224 and 234. At least one of pull-up output transistors 220 and 232 and one of pull-down output transistors 224 and 234 should be programmed to provide DC current. In this manner, users can select different strengths for the DC and AC currents separately, thereby achieving a fast edge rate with a relatively small output voltage swing.

Figure 2B is a timing diagram for an exemplary operational case of the circuit 100 of Figure 2A. Refer to both Figure 2A and Figure 2B. In this exemplary case, the DC output is enabled. In this case, the configuration bit 202 (Figure 2A) is high; configuration bit 204 is low; enable 104 is high; enable 103 is high; the C and D inputs of OR gate 212 are low and the F input of AND gate 216 is high. Waveform 251 represents transitions on the input 102. Waveform 252 represents transitions on the output of the inverter circuit coupled to receive input 102. Waveform 253 represents transitions on the input to output transistor 220. Waveform 254 represents transitions on the output transistor 224. Waveform 255 represents transitions on the output 114.

The falling edge of 252 causes the falling edge of both 253 and 254. The falling edge of 253 starts the rising edge of output data signal 255 and the rising edge of 254 starts the falling edge of output data signal 255.

According to this operational mode, if configuration bit 202 is programmed high, then transistor 220 will be on as long as the input signal 102 is high, providing a continuous output current which would contribute to the DC output voltage swing.

Figure 2C is a timing diagram of the AC booster control rising edge circuit 106 for an exemplary operational case of the circuit 100 of Figure 2A. Refer to both Figure 2A and Figure 2C. In this exemplary case, the AC booster control circuit 106 is enabled while output transistors 232 and 234 are programmed to provide DC output current.

In this case, the configuration bit 202 (Figure 2A) is low; configuration bit 204 is high; enable 104 is high; enable 103 is high; and the D input of OR gate 212 is low. Waveform 256 represents input B of NOR gate 210. Waveform 257 represents input C of OR gate 212. Waveform 258 represents input E of NAND gate 214. Waveform 259 represents input F of AND gate 216. Waveforms 251-255 are analogous to those circuit points as described with reference to Figure 2B.

In operation, if bit 202 is low, then transistor 220 will be ON only during the transition time when the input 102 is switching from low to high; the duration of this ON time can be programmed by the programmable delay element 206. This short period of current through transistor 220 will charge up the loading on the output pin and reduce the rise time, but will not generally affect the DC output voltage swing.

Similarly, transistor 224 can be totally disabled when enable 103 is low, or programmed to provide a DC output current if enable 103 is high and 204 is low, or further, programmed to be ON only when the input is switching from high to low. The programmable delay 208 controls the duration of the ON state.

DIFFERENTIAL EMBODIMENT

The programmable current booster according to the embodiment of the present invention described above for a single-ended output driver may also be applied in a differential output driver. Differential drivers are used to implement differential signals which are carried on

pairs of conductors in which the signals propagate in parallel. Differential signals are opposite in polarity and referenced relative to each other, rather than to ground.

FIG. 3 is a preferred implementation of a differential output driver 700 according to one embodiment of the present invention. Output transistors 516, 518, 528 and 530 provide DC output current, while output transistors 522, 523, 520 and 521 are AC current boosters. DC stage rising edge control circuits 510 have the analogous delay as the AC booster control circuits 106, so the DC and AC currents are switched on simultaneously. The control circuits 106 for current-regulating output transistors 520 and 522 in this differential embodiment are identical to that of circuit 106 for the single-ended case of FIG. 2A. Similarly, control circuits 110 for output transistors 521 and 523 are identical to that of circuit 110 for the single-ended case of FIG. 2A.

The differential output driver of FIG.3 may optionally use the current and voltage regulating arrangement depicted as voltage source (Vcc) 524 in series with current regulator 536, and current regulator 538 coupled to Ground, for supplying current to differential outputs 506 and 508. This permits the differential output signal to be further conditioned to fall within upper and lower limits of current and voltage in accordance with the applicable differential signaling standard.

FIG. 4 shows exemplary details of a preferred circuit implementation of the differential DC stage rising edge

control circuit 510 for the differential embodiment 700 of Figure 3. The OR gate 602 has a first OR input from the common input or data signal 502/504 received from the integrated circuit device, a second OR input from an input/ output configuration signal 514 ("enable signal") received from the integrated circuit device and inverted via an inverter circuit, and a third OR input coupled to the second OR input (e.g., also from the output of the inverter circuit). Output transistor 516/518 of Fig. 3 is coupled to the output of OR gate 602.

In operation of circuit 510, if the enable signal 514 is low, then the output of the OR gate 602 is forced high regardless of the data input pin 502/504 once the inverter signal output becomes stable. If the enable signal 514 is high, then the output of the OR gate 602 will track the data input value 502/504, again, once the output of the inverter is stable.

The DC stage rising edge control circuits 510 should be designed to have the same delay as the rising edge AC booster control circuits 106, so the DC and AC currents are switched on simultaneously. Alternately, rising edge control circuit 106, once programmed to provide DC current, can be used to control output transistors 516/ 518, again providing simultaneous switching on for the DC and AC currents.

FIG. 5 shows exemplary details of a preferred circuit implementation of the differential DC stage falling edge control circuit 512 for the differential embodiment 700 of Figure 3. The AND gate 702 is coupled to receive a first

AND input from the common input signal 502/504 received from the integrated circuit device, a second AND input from an input/output configuration signal 514 ("enable signal") received from the integrated circuit device, and a third AND input coupled to the second AND input. Output transistor 528/530 are coupled to receive the output of AND gate 702.

In operation of circuit 512, if the enable signal 514 is low, then the output of the AND gate 702 is forced low regardless of the data input pin pair 502/504. If the enable signal 514 is high, then the output of the AND gate 702 will track the data input value 502/504.

The DC stage falling edge control circuit 512 should be designed to have the same delay as the AC booster control circuits 110, so the DC and AC currents are switched on simultaneously. Or alternately, falling edge control circuit 110, once programmed to provide DC current, can be used to control output transistors 528 and 530, whereby the DC and AC currents will be switched on simultaneously.

Figure 6 is a timing diagram for an exemplary operational case of the circuit 700 of Figure 3. Refer to both Figure 3 and Figure 6. In this case, enable 532, enable 534 and enable 514 are all high; input 202 (of AC booster control block 106) is low and configuration bit 204 (of falling edge control block 110) is high. Waveform 610 represents input 502. Waveform 615 represents the output of the inverter that receives input 502. Waveform 620 represents input 504. Waveform 625 represents the output of the inverter that receives input 504. Waveform 630 represents

the gate signal at output transistors 516 and 528. Waveform 635 represents the gate signal at output transistors 518 and 530. Waveform 640 represents the gate signal for transistor 522. Waveform 645 represents the gate signal for transistor 523. Waveform 650 represents the gate signal for transistor 520. Waveform 655 represents the gate signal for transistor 521. Waveforms 660 and 665 represent the differential output signals 506 and 508, respectively.

In operation, output transistors 516, 528, 518 and 530 provide DC output current, while transistors 522, 523, 520 and 521 are AC current boosters. The control circuit for the DC output transistors is designed to have the same delay as the AC booster control circuits, so the DC current and AC current will be switched on at the same time.

While specific circuits have been used to describe the present invention, the idea of using a programmable current booster in an integrated circuit output driver, with programmable duration and programmable strength of the AC booster current may be implemented using other circuit embodiments. It is intended that the invention not be limited to the particular embodiments disclosed, but that the invention will include all embodiments and all equivalents falling within the scope of the claims.

What is claimed is: